Abstract of the Disclosure

A method for estimating noise in an integrated circuit substrate. A model file is created for a technology process for fabricating the integrated circuit. Noise generated by a digital circuit and input/output circuitry to be implemented in the integrated circuit are estimated. A substrate netlist is generated for the integrated circuit. A floorplan is determined for the integrated circuit. Transient simulations are run with predetermined input values. Finally, it is determined if predetermined noise requirements are met in results of the transient simulations.